In the claims:

1. (previously presented) A method for handling operations within a hardware device, comprising:

providing within the device information regarding an operation, the operation having a predetermined responsive output as encoded within a transaction lookup table and an alternative responsive output stored in a register, the provided information including information identifying the operation;

selecting at least some of the identifying information of the operation to output to a comparator and the transaction lookup table, by employing a masking register that filters the at least some of the identifying information of the operation for output to the comparator, the masking register being logically AND'ed with all the identifying information of the operation and having binary ones corresponding to the at least some of the identifying information to output to the comparator and binary zeros corresponding to other of the identifying information not output to the comparator, output of the comparator and output of the transaction lookup table being input into a multiplexer;

selecting the alternative responsive output for the operation instead of the predetermined responsive output based upon the comparator comparing the selected identifying information to the operation resulting in a match between the selected identifying information and the operation directing the multiplexer to output the alternative responsive output, such that the multiplexer effectively converts at least some of the information regarding the operation based upon the selected identifying information; and

executing the operation based upon the converted information.

2. (original) The method of claim 1, wherein the provided information is within a register of the device.

3. (original) The method of claim 1, wherein the identifying information is within a register of the device.

4. (original) The method of claim 1, wherein the converted information is within a register of the device.

5. (previously presented) The method of claim 1, wherein the step of providing information regarding the operation comprises providing the predetermined responsive output and the alternative responsive output.

6. (cancelled)

7. (original) The method of claim 5, wherein the operation identifications comprise fields for operation identification, length, attribute and target of each operation.

8. (previously presented) A method for redirecting transactions within a hardware device, wherein transactions occurring within said device contain fields of information regarding the transaction, the method comprising the steps of:

loading all of said fields necessary to identify a transaction into a first register;

selecting which fields of said first register are to be acted upon and inputting the selected fields into a multiplexer, the fields of said first register selected by employing a masking register that filters the fields of said first register, the masking register being logically AND'ed with the said first register and having binary ones corresponding to the fields being selected and binary

zeros corresponding to the fields not selected;

converting the transaction information to be redirected through a pre-programmed value for each said field by inputting into the multiplexer a predetermined responsive value into the multiplexer, the predetermined responsive value stored in a transaction lookup table, and an alternative responsive output stored in the first register, such that the multiplexer receives the alternative responsive output as input from the first register, the multiplexer also receiving input from a comparator, such that the multiplexer outputs the alternative responsive value for the transaction based upon the comparator comparing the selected fields to the transaction resulting in a match; and

outputting corrected transaction results, as one of the predetermined responsive value and the alternative responsive output.

9. (cancelled)

10. (original) The method of claim 8, wherein said fields of information are comprised of a field for transaction identification, length, attribute and target of each transaction.

11. (previously presented) A method for redirecting operations within a hardware device, wherein operations occurring within said device contain fields of information regarding the operation and such operations are compared with a preprogrammed list of responses and the hardware device issues responses based on each operation, the method comprising the steps of:

creating a list of identified operations for which a redirected response is desired, the redirected response stored in a register and the preprogrammed list of responses stored in a transaction lookup table;

comparing an operation with the list of said identified operations using a comparator, the operation compared using the comparator by first employing a masking register that filters at least

some of identifying information of the operation for use by the comparator, the masking register being logically AND'ed with all the identifying information of the operation and having binary ones corresponding to the at least some of the identifying information for use by the comparator and binary zeros corresponding to other of the identifying information not used by the comparator;

outputting match results of the comparator and a preprogrammed response from the preprogrammed list of responses for the operation into a multiplexer, such that output of the multiplexer represents the redirected response for the operation; and

substituting the redirected response for the preprogrammed response from said preprogrammed list of responses.

12. (previously presented) The method of claim 11, wherein the step of creating a list of identified operations includes first loading transaction identification.

13. (original) The method of claim 11, wherein said fields of information are comprised of a field for transaction identification, length, attribute and target of each transaction.

14. (previously presented) In a data processing system in which a given operation results in a predetermined response, a system for altering such predetermined response comprised of:

first storage means to identify operations for which a response different from said predetermined response is desired;

comparator means to compare said given operation with said identified operations, the given compared using the comparator means by first employing a masking register that filters at least some of identifying information of the operation for use by the comparator means, the masking register being logically AND'ed with all the identifying information of the operation and having binary ones corresponding to the at least some of the identifying information for use by the

comparator means and binary zeros corresponding to other of the identifying information not used by the comparator means;

second storage means to load a substitute response for said predetermined response, the second storage means comprising a plurality of registers, the substitute response stored in a register and the predetermined response stored in a transaction lookup table; and

selection means to select said substitute response when a given operation meets a predefined criteria for substituting a response from said second storage means, the selection means comprising a multiplexer into which the predetermined response is input and output from the plurality of registers is input, such that output of the comparator means is employed to select the output of the plurality of registers in lieu of the predetermined response as the substitute response.

15. (original) The system of claim 14, wherein one or more of said storage means may be selectively enabled or disabled.

16. (previously presented) In a data processing system utilizing a hardware control device in which a given operation results in a predetermined response for that operation, a system for providing a programmable redefinition of allowed instructions and associated responses within said hardware device including:

first register means which contains fields to identify preselected operations which may occur within the system;

second register means which operates upon selected fields in the first register means to further define a criteria for which redirecting a response is desired, the second register means being a masking register that filters the selected fields of the first register means, the masking register being logically AND'ed with all the fields of the first register means and having binary ones corresponding to the selected fields and binary zeros corresponding to other of the fields;

comparator means which compares the identified operations with a current operation;

transaction lookup table means to output a standard value for the current operation; and

multiplexer means receiving input from the comparator means and the transaction lookup table means and outputting a substitute value for a predetermined value for the current operation, the substitute value stored in a register and the predetermined value stored in a transaction lookup table.

17. (original) The system of claim 16, wherein one or more of said register means may be selectively enabled or disabled.

18. (previously presented) A data processing system for executing an operation, comprising:

an identification store including information identifying at least selected operations by employing a masking register that filters at least some of the information of the selected operations, the masking register being logically AND'ed with all the information of the selected operations and having binary ones corresponding to the at least some of the information and binary zeros corresponding to other of the information of the selected operations;

a comparator responsive to the operation and the identifying information;

a substitute value responsive to the comparator and the operation and stored in a register;

a standard value responsive to the comparator and the operation and stored in a transaction lookup table; and

a multiplexer into which the substitute value, the standard value, and output from the comparator are input, and that outputs one of the substitute value and the standard value based on the output from the comparator.

19. (original) The system of claim 18, wherein the comparator is responsive to a mask of the identifying information.